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Claims

[c1] A conductor line stack, comprising:
a layer of a first material;
a layer of a second material formed on said layer of first material, said layer of second material having an upper portion and a lower portion; and
a pair of first spacers disposed on sidewalls of said upper portion, said lower portion having width defined by a combined width of said upper portion and said pair of first spacers.

[c2] The conductor line stack of claim 1 wherein said first material includes a material selected from the group consisting of polysilicon and a metal silicide.

[c3] The conductor line stack of claim 2 wherein said second material includes a metal.

[c4] The conductor line stack of claim 1, wherein said conductor line stack further comprises an insulating cap disposed over said layer of second material, and second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said layer of said first material.

[c5] A conductor contact structure including a conductor line stack as claimed in claim 4, further comprising a borderless bitline contact to a single-crystal semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

[c6] A conductor contact structure including a pair of conductor line stacks as claimed in claim 4, said conductor line stacks being oriented in parallel, said conductor contact structure further comprising a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks.

[c7] The conductor contact structure of claim 6 wherein said borderless bitline contact includes heavily doped polysilicon.

[c8] The conductor contact structure of claim 7 wherein said borderless bitline contact includes a layer of metal silicide disposed above said heavily doped polysilicon.

[c9] The conductor contact structure of claim 8 wherein a conductor line stack of said pair is separated from said single-crystal semiconductor region by an array top ox-

ide layer and another conductor line stack of said pair is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

[c10] A conductor contact structure comprising:
a pair of conductor line stacks oriented in parallel, each said conductor line stack including:
a layer of a first material selected from the group consisting of heavily doped polysilicon and a metal silicide;
a layer of metal formed over said layer of first material, said layer of metal having an upper portion and a lower portion;
an insulating cap formed over said layer of metal; and
a pair of first spacers disposed on sidewalls of said upper portion and said insulating cap, said lower portion having width defined by a combined width of said upper portion and said pair of first spacers; and
a pair of second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said layer of first material;
a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks,
wherein a conductor line stack of said pair is separated

from said single-crystal semiconductor region by an array top oxide layer and another conductor line stack of said pair is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

[c11] A method of fabricating a conductor line stack for an integrated circuit, comprising:
forming a layer of a first material;
forming a layer of a second material on said layer of first material, said layer of second material having a lower portion contacting said layer of first material and an upper portion disposed above said lower portion;
photolithographically patterning said upper portion;
forming a pair of first spacers on sidewalls of said upper portion;
etching said lower portion and said layer of first material while using said first spacers as a mask; and
forming a second pair of spacers on sidewalls of said first spacers, said lower portion and said layer of first material.

[c12] The method of claim 11 wherein said first material includes at least one material selected from the group consisting of polysilicon and a metal silicide.

[c13] The method of claim 12 wherein said second material in-

cludes a metal.

[c14] The method of claim 11 further comprising forming an insulating cap over said layer of second material prior to photolithographically patterning said upper portion.

[c15] A method of forming a conductor contact structure including forming a conductor line stack according to the method claimed in claim 14, further comprising forming a borderless bitline contact to a single-crystal semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

[c16] A method of forming a conductor contact structure including forming a pair of conductor line stacks according to the method claimed in claim 14, further comprising orienting said pair of conductor line stacks in parallel, and forming a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said pair of conductor line stacks.

[c17] The method of claim 16 wherein said step of forming said borderless bitline contact includes depositing heavily doped polysilicon onto said single-crystal semicon-

ductor region.

[c18] The method of claim 17 wherein said step of forming said borderless bitline contact includes forming a layer of metal silicide contacting said heavily doped polysilicon.

[c19] The method of claim 18 further comprising providing an array top oxide layer separating at least one of said pair of conductor line stacks from said single-crystal semiconductor region.

[c20] The method of claim 19 further comprising conductively coupling at least one of said pair of conductor line stacks to a gate conductor of a vertical passgate transistor of a dynamic random access memory.